REMARKS

Applicants respectfully request reconsideration of the subject application, as amended. Claims 5 and 16 have been canceled without prejudice. Claims 1-4, 6-15 17 and 18 have been amended and are still pending in the application.

The Examiner has objected to the Specification, in that the title of the invention is not is not descriptive. Applicants request the Examiner to accept the amended title of which is "Mos Transistor Using Mechanical Stress to Control Short Channel Effects." Furthermore, the Examiner has objected to the Abstract as not being clearly indicative of the invention claimed to which the claims are directed. Applicants are submitting a new Abstract of the Disclosure under a separate cover. Applicants respectfully request the Examiner to accept the substitute Abstract of the Disclosure. Accordingly, Applicants respectfully request the Examiner to withdraw the objection to the Specification.

The Examiner has rejected claims 1, 2, 5-9, 13, 15 and 17 under 35 U.S.C. § 102(e) as being anticipated by Kokubun (U.S. Patent 6,248,652). Furthermore, the Examiner has rejected claims 3, 4, 14, 16, and 18 under 35 U.S.C. § 103(a) as being unpatentable over Kokubun and/or the combination of Kokubun in view of Akatsu et al. (U.S. Patent 6,329,271) or Adan (U.S. Patent 6,288,425). Applicants submit that the amended independent claims 1, 8 and 15 now recite allowable subject matter, placing all of the pending claims in condition for allowance. Specifically, Kokubun fails to disclose use of voids to place mechanical stress (compressive or tensile stress) to alter carrier mobility in a region. Kokubun, along with the other relied upon references of Akatsu et al. and Adan, fail to disclose this aspect of the claimed embodiments of the invention. Accordingly, Applicants

respectfully request the Examiner to withdraw the 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a) rejections as noted in the current Office Action.

Accordingly, Applicants submit that pending claims 1-4, 6-15, 17 and 18, as amended, are in condition for allowance.

Please charge any additional fees due, if any, to Deposit Account 02-2666.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please replace the title with the following:

--MOS TRANSISTOR USING MECHANICAL STRESS TO CONTROL SHORT CHANNEL EFFECTS--

Please amend the paragraph starting at page 1, line 5 with the following:

[0001] This is a divisional application of Serial No. 09/342,030 filed June 28, 1999 [that is currently pending], now U.S. Patent 6,362,082.

IN THE CLAIMS

1. A [apparatus] transistor device, comprising:

a substrate having a source region, a drain region[,] and a channel region [having], in which at least one of the source, drain and channel regions has a void to [provide a barrier to lines of force to reduce leakage current] place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress; and

a gate region formed over the channel region.

2. The [apparatus] transistor of claim 1 wherein [said] the void is located substantially in a center of [said] the channel region.

11. The [apparatus] transistor of claim 1 wherein [said] the void is approximately 50 nm across.

12. The [apparatus] transistor of claim 3 wherein [said] the void is located at a depth of approximately 1000 angstroms in [said] the channel region.

13. Please cancel claim.

14. The [apparatus] transistor of claim [5] 1 wherein [said] the void is located in the channel region and near an edge of [said] the channel region adjacent to [said] the source region.

15. The [apparatus of 6 further comprising a] transistor of claim 1 wherein the void is located in the channel region near an edge of the channel region adjacent [said] to the drain region.

16. A[n apparatus] transistor, comprising:

[a gate region; and]

a substrate having a source region, a drain region[,] and a channel region, [and] in which a void is located below [said] the source region to [provide a barrier to lines of force to reduce leakage current] place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress; and

a gate region above the channel region.

17. The [apparatus] transistor of claim 8 wherein a void is also located below [said] the drain region.

18. The [apparatus] transistor of claim 9 wherein [said] the source and drain regions [and said drain region] are under compressive stress.

15. The [apparatus] transistor of claim 8 wherein [said] the source region is under tensile stress.

16. The [apparatus] transistor of claim 8 wherein [said] the drain region is under compressive stress.

17. The [apparatus] transistor of claim 8 wherein [said] the gate region is polysilicon.

18. The [apparatus] transistor of claim 8 wherein [said] the gate region is metal.

15. A[n apparatus] transistor comprising

[a gate region having a void to provide a barrier to lines of force to reduce leakage current; and]

a substrate having a source region, a drain region[,] and a channel region; and.

a gate region having a void to place the substrate under mechanical stress to alter carrier mobility due to the stress.

16. Please cancel claim.

18. The [apparatus] transistor of claim 15 wherein [said] the gate region is polysilicon.

18. The [apparatus] transistor of claim 15 wherein [said] the gate region is metal.